



Molding Functional Coverage and Reporting for Highly Configurable IP

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Agenda

Background and Problem

Our Approach

Coverpoints are not in a vacuum

Mode-of-operation

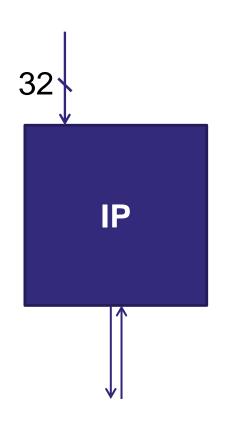
DUT Configuration

"The Demo" or "What this looks like without actually running a demo"

Some Serial Controller IP





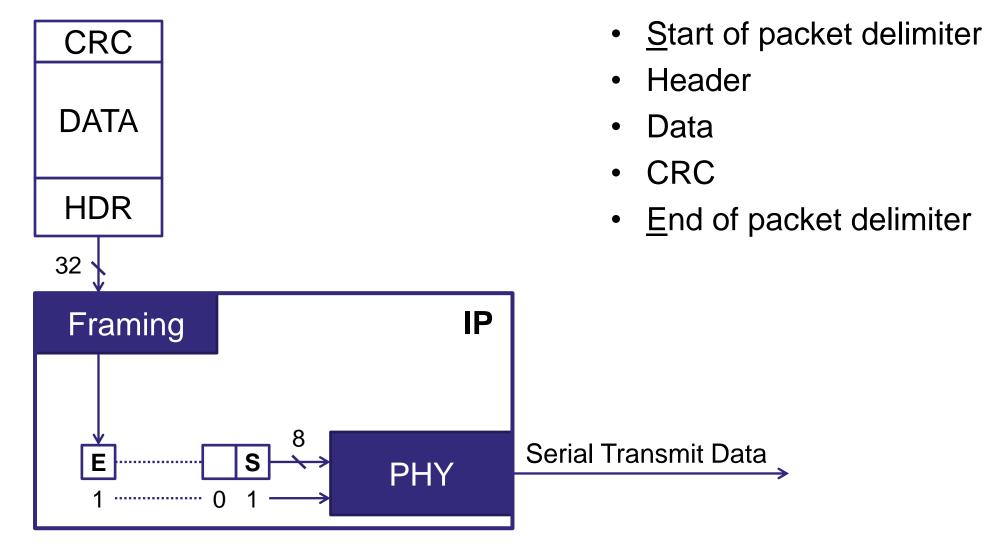


- Data path is 32 bits
- Single lane transmit/receive
- Generation 1 speed

Packet Data





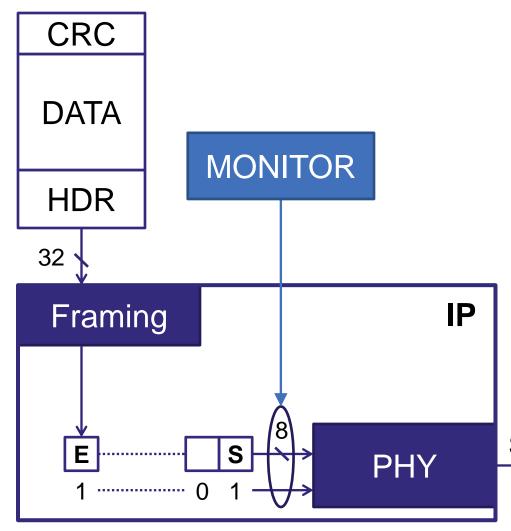


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Packet Data







- Monitor delimiters
- Start of packet depends on origin
 - STP = start transport packet (8'hFB)
 - SDP = start data link packet (8'h5C)
- End of packet depends on data
 - END = good packet (8'hFD)
 - EDB = bad/nullified packet (8'hFE)

Serial Transmit Data

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Monitor





- No correlation
 - data == 8'hFE when ctrl == 0
 - False positive for EDB coverage

- Over-correlated
 - data == 8'hFE && ctrl == 1
 - EDB covered!

Obviously, not the way to do functional coverage

T also hogalive for invalid control character

Monitor





<u>G</u>oldi<u>L</u>ocks

```
class MonitorGL;
  logic [7:0] data;
                           // 8-bit data path
                           // 1-bit control path
  logic ctrl;
  covergroup tx_dp_cg;
    coverpoint data {
       bins data_0[] = {
          8'hFB, 8'h5C, 8'hFD, 8'hFE };
    coverpoint ctrl {
       bins ctrl_0 = { 1'b1 };
    c_0: cross data, ctrl {
       delim_cross =
          binsof(data.data_0) &&
          binsof(ctrl_0);
  endgroup
endclass
```

- Properly correlated covergroup
- When cross c_0 is covered, the whole group is covered

Only care about delimiter encodings

Only when characters are marked as control

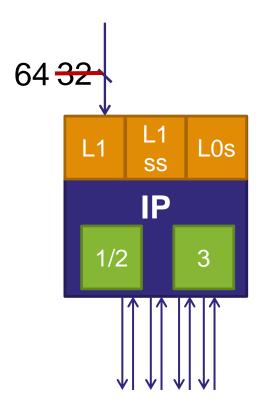
Sample only packet delimiter control characters

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General PCIe Controller IP

= \$\$ for company

= Job for me







64

Data path is 💥 bits

Four

Single lane transmit/receive
 Two

Generation x speed



3

Low power support



L0s

— L1

L1 Sub-states

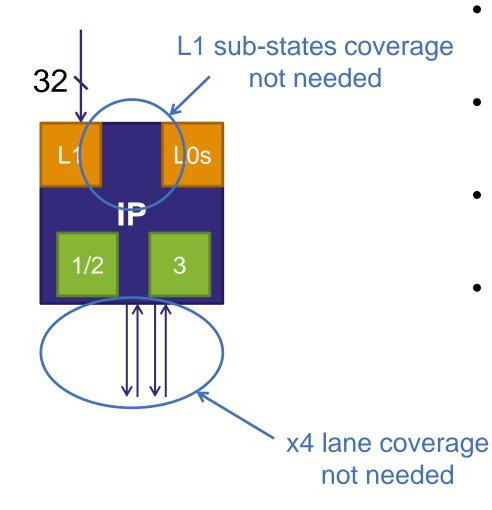


PCIe Controller IP





Gen3, 2-Lane, Low Power L0s and L1 support

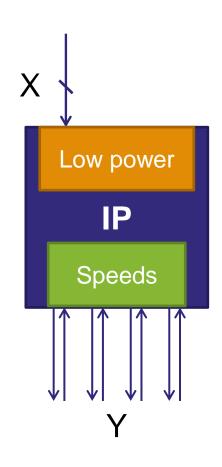


- Data path is 32 bits
- Two lane transmit/receive
- Generation 3 speed
- Low power support
 - L0s
 - L1

General PCIe Controller IP







Data path is X bits

Config – Fixed value

Y number of lanes transmit/receive

Config – Supported at compile-time

Mode – Enabled at runtime

Generation Z speed

Config – Supported at compile-time

Mode – Enabled at runtime

Low power options include/exclude

Config – Supported at compile-time

Mode – Enabled at runtime

Monitor





```
class MonitorGL;
  logic [7:0] data;
                           // 8-bit data path
  logic ctrl;
                           // 1-bit control path
  covergroup tx_dp_cg;
    coverpoint data {
       bins data_0[] = {
          8'hFB, 8'h5C, 8'hFD, 8'hFE };
    coverpoint ctrl {
       bins ctrl 0 = \{ 1'b1 \};
    c_0: cross data, ctrl {
       delim_cross =
          binsof(data.data_0) &&
          binsof(ctrl_0);
  endgroup
endclass
```

- Are all delimiters covered when:
 - GEN1, GEN2, GEN3 speed?
 - x1 support: x1 enabled?
 - x2 support: x1 enabled, x2 enabled?
 - x4 support: x1, x2, x4 enabled?
 - Lanes reversed?
 - Lane polarity reversed?
 - After transition out of L0s?
 - After transition out of L1?
 - After transition out of an L1 sub-state?

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Monitor





class

Odi

Customer 2: Did you even test this mode?

ers covered when:

GEN3 speed?

covergroup tx_dp_cg;

ctrl

The coverage scenario questions are applicable to ALL covergroups

Shape group based on config

data
oss =
f(dat
f(ctrl)

data
oss =
f(dat
f(ctrl)

of
operation

- Lanes reverseur
- Lane polarity reversed?
- After transition out of L0s?

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Customer 1:
I see an error when ...!





Agenda

Background

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Mode-of-operation

DUT Configuration

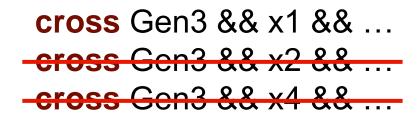
"The Demo" or "What this looks like without actually running a demo"

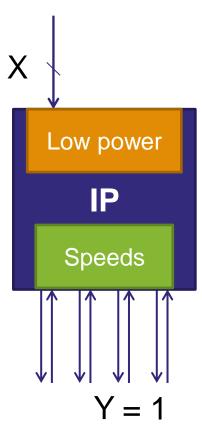
Customer 2: Did you even test this mode?





- Mode-of-operation
 - Selected once or a few times during simulation
 - Often only at the beginning of simulation
 - Affects coverage context
- Configuration
 - Selected via `defines throughout the RTL
 - Affects structure of covergroup





Goals





- Write covergroups once
- Automatically shape all covergroups by configuration
- Automatically propagate mode coverpoints to covergroups

Avoid waivers at (nearly) all costs

When cross c_0 is covered, the whole group is covered

Table Format





```
Coverpoints Data Ctrl

8'hFB 8'h5C binsof(data.data_0) && binsof(ctrl.ctrl_0);

coverpoint data {
bins data_0[] = {
8'hFB, 8'h5C, 8'hFD, 8'hFE};
}

coverpoint ctrl { bins ctrl_0 = { 1'b1 }; }
```

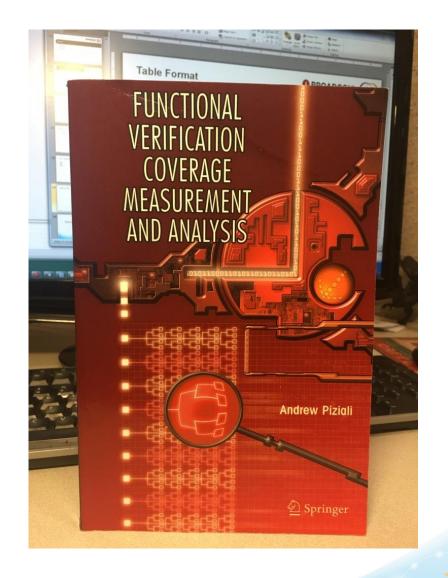


Table Format





Coverpoints	Data	Ctrl
c_0	8'hFB, 8'h5C 8'hFD, 8'hFE	1

•	Write	covergroup	once

- Automatic mode propagation
- Shape based on configuration

How to setup mode propagation?

Coverpoints	Data	Ctrl	M_Speed	M_Width
c_0	8'hFB, 8'h5C 8'hFD, 8'hFE	1	G1, G2	x1, x2, x4

Z = G1, G2 Y = x1

Coverpoints	Data	Ctrl	M_Speed	M_Width
c_0	8'hFB, 8'h5C 8'hFD, 8'hFE	1	G1, G2	x1

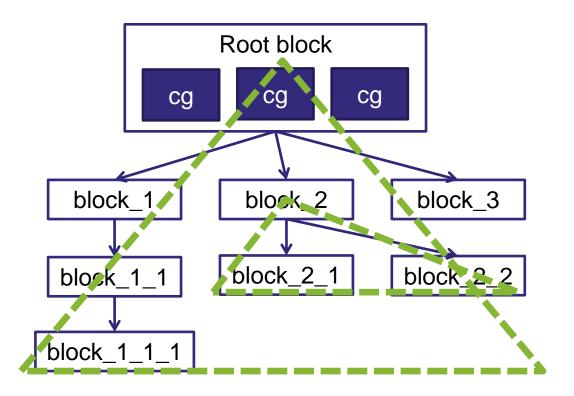
How filter based on configuration?

Hierarchical Abstract Model





- Cover block
 - Collection of related cover groups and cover blocks
- Block model
 - Sub-tree from any block
- Cover model
 - Sub-tree from the root block

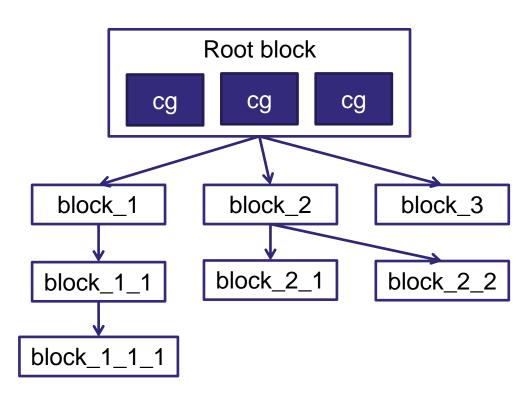


Hierarchical Abstract Model





- Cover block
 - Collection of related cover groups and cover blocks
- Block model
 - Sub-tree from any block
- Cover model
 - Sub-tree from the root block
- Cover block Excel Spreadsheet
- Cover model Directory structure



Cover Variables





Cover

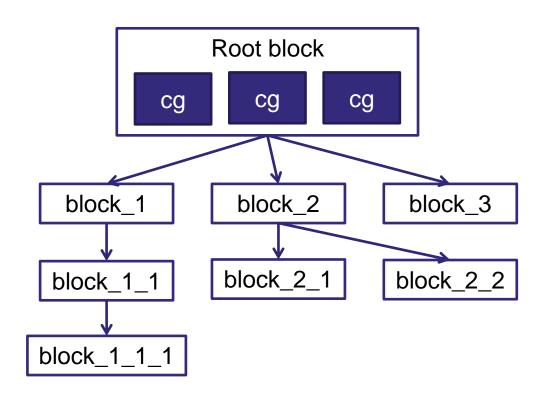
encourage reuse

Mode

 special case cover variable automatically propagated to all covergroups in the current coverblock and child coverblocks

Config

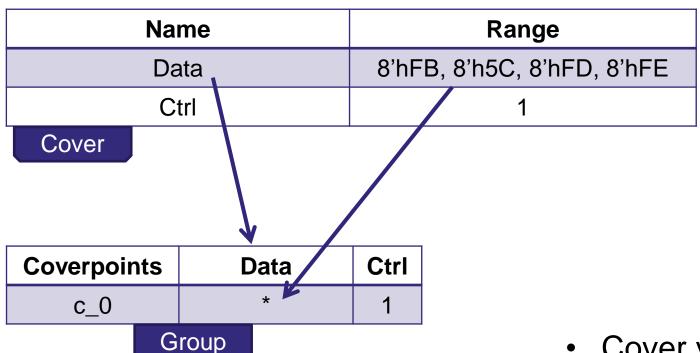
 special case cover variable used to filter mode variable values AND cover group scenarios



Cover variables in block_1







root/block_1/Cover.xlsx

- Cover variables may be re-used:
 - In current spreadsheet
 - In any child block's spreadsheet

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Config and Mode variables in Root





Name	Range
C_Speed	G1, G2, G3
C_Width	x1, x2, x4

Config

Mode

Name	Range
M_Speed	G1, G2, G3
M_Width	x1, x2, x4

root/Cover.xlsx

- Mode variables are propagated to:
 - Current spreadsheet cover groups
 - All child blocks' spreadsheet cover groups

Specific configuration

Supported speeds: G1, G2; Support width: x1





Name	Range
C_Speed	G1, G2, G3
C_Width	x1, x2, x4

Config

Name	Range
M_Speed	G1, G2, G3
M_Width	x1, x2, x4

root/Cover.xlsx

Mode

- Config variables filter:
 - All mode variables
 - Any cover group scenario that specifies it

Specific configuration

BROADCOM® connecting everything ®



Supported speeds: G1, G2; Support width: x1

Name	Range
C_Speed	G1, G2
C_Width	x1
Config	

Name	Range
M_Speed	G1, G2, G3
M_Width	x1, x2, x4

root/Cover.xlsx

Mode

- Config variables filter:
 - All mode variables
 - Any cover group scenario that specifies it

Specific configuration





Supported speeds: G1, G2; Support width: x1

Name	Range	
C_Speed	G1, G2	Assumed named value
C_Width	x1	(i.e. enumeration)
Config		root/Cover.xlsx
Name	Range	TOOU OOVCI.XISX
M_Speed	G1, G2	
M_Width	x1 🖊	
Mode		

- Config variables filter:
 - All mode variables
 - Any cover group scenario that specifies it

Cover variables in block_1





Name	Range
C_Speed	G3
C_Width	x1
Config	

root/Cover.xlsx

Coverpoints		Data		Ctrl			C_Speed	
2.0		*		4			C4 C2	
0_0	0_0				ı		01, 02	
	Groui	0		-		-		

Not applicable Removed

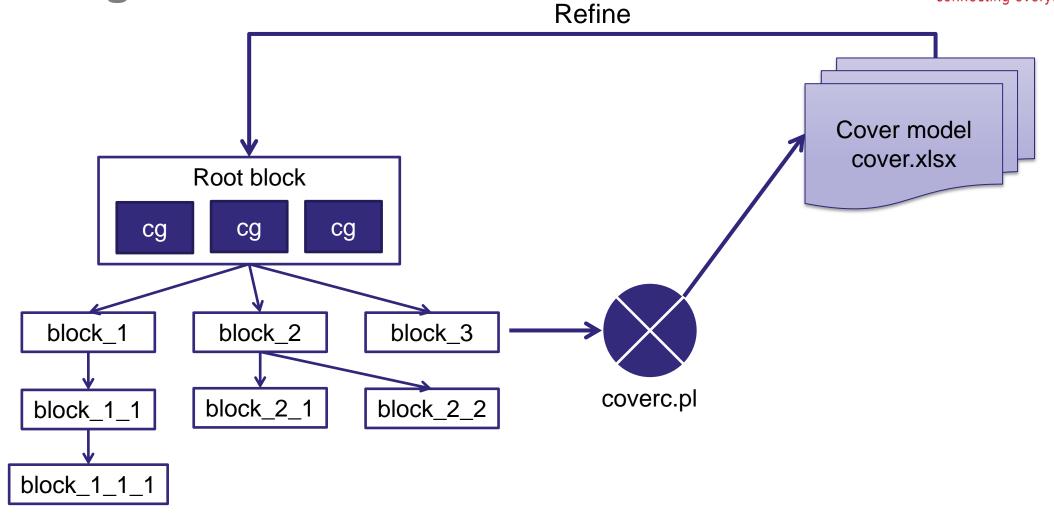
root/block_1/Cover.xlsx

- Config variables filter:
 - Any cover group scenario that specifies it

SNUG 2016 26

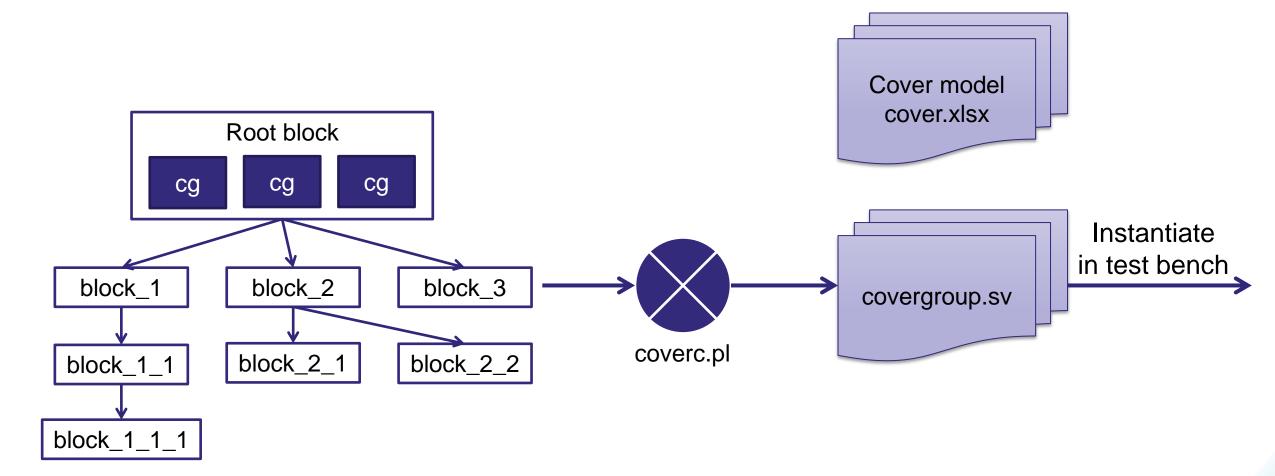






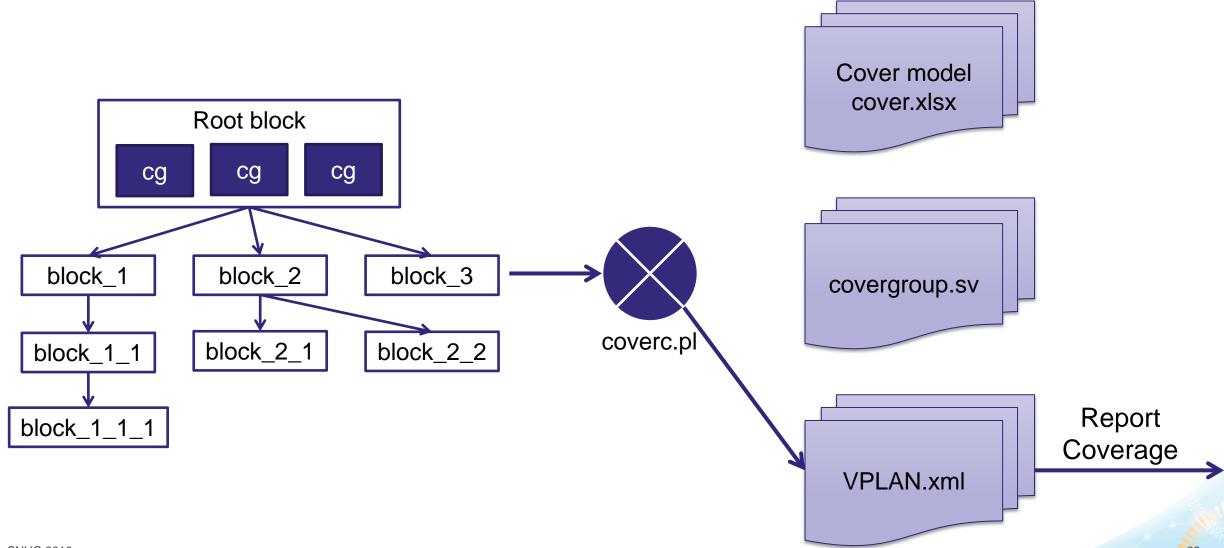






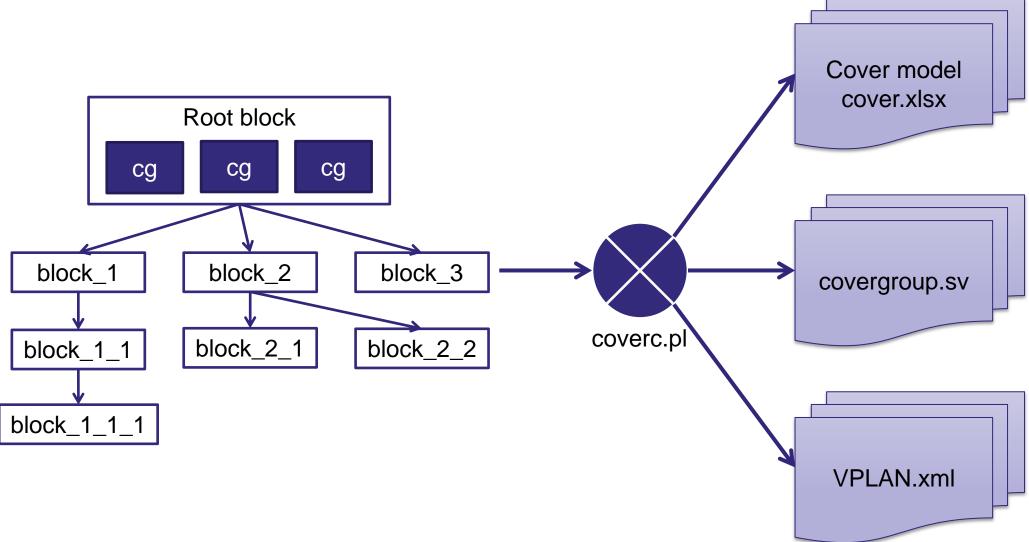
















Agenda

Background

Our Approach

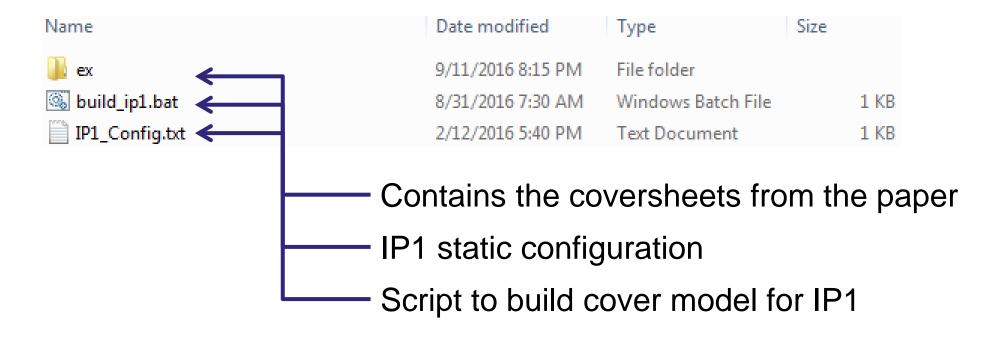
"The Demo" or "What this looks like without actually running a demo"

Coversheet examples from the paper

Root Cover Model Directory







Root Cover Block





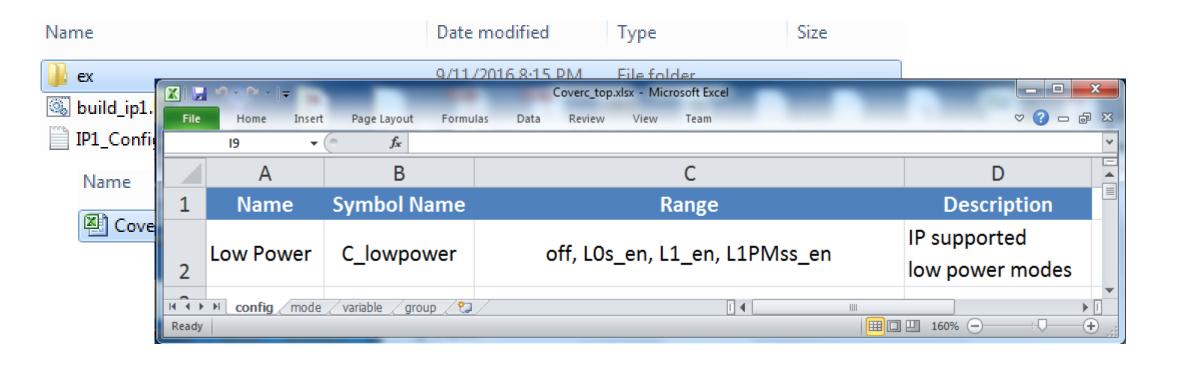
Name	Date modified	Type	Size
🔐 ex	9/11/2016 8:15 PM	File folder	
uild_ip1.bat	8/31/2016 7:30 AM	Windows Batch File	1 KB
IP1_Config.txt	2/12/2016 5:40 PM	Text Document	1 KB
Name	Date modified	Туре	Size
Coverc_top.xlsx	8/31/2016 7:29 AN	Microsoft Excel W	13 KB
	Root block cover	sheet	

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Root Block::Config Tab





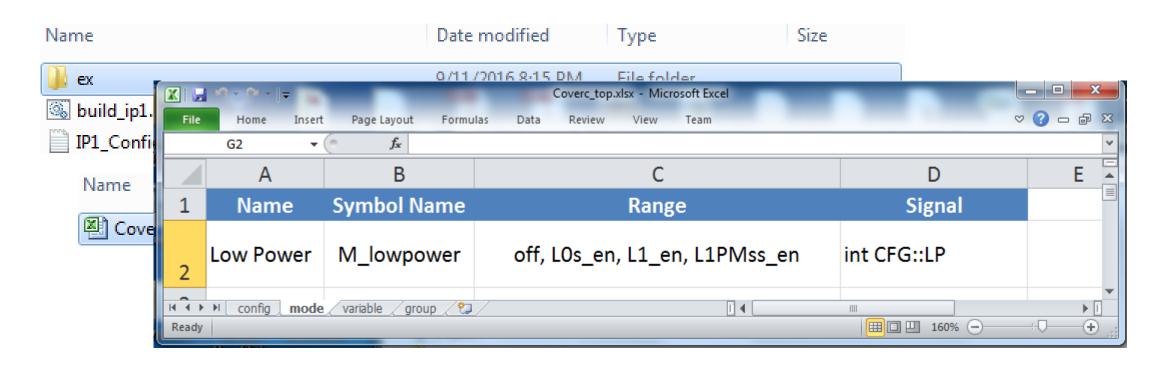


- config tab lists configuration variables
- Identifies static (compile-time) configuration values for the DUT

Root Block::Mode Tab







- mode tab lists mode variables
- Mode variable range values are pass-thru filtered by config variables

Root Block::Variable Tab





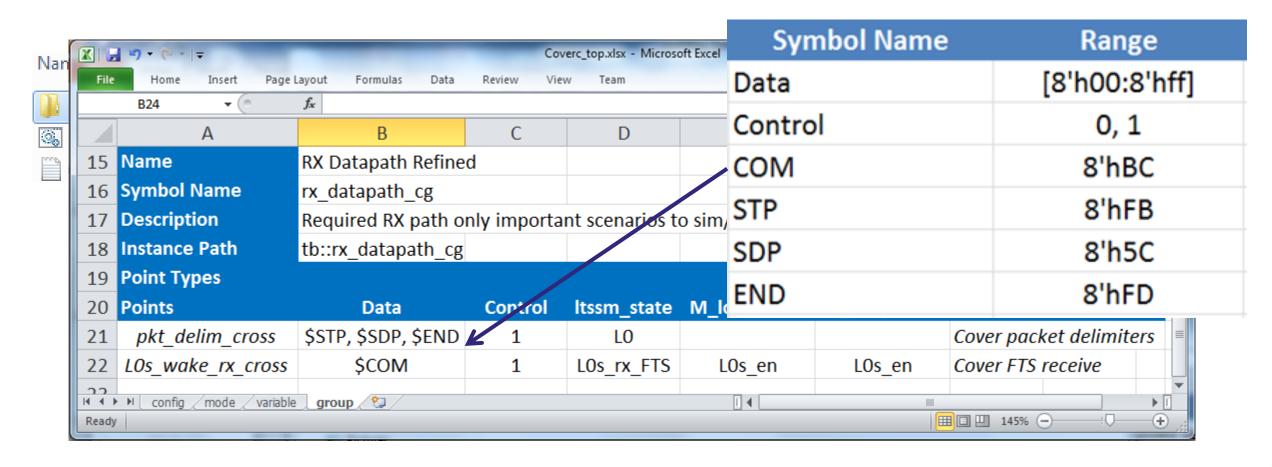
	Coverc_top.xlsx - Microsoft Excel Coverc_top.xlsx - Microsoft Excel							
	File	Home Insert Page	Layout Formulas Data Re	view View Team		♡ ② □ @ ♡	3	
Name	A10 • (**)						~	
		А	В	С	D	E		
<u></u> ex	1	Name	Symbol Name	Range	Signal	Description		
S build_	2	Data	Data	[8'h00:8'hff]	data	Decoded data bus from DUT		
IP1_Cd	3	Control	Control	0, 1	ctrl	Control character indication		
Name	4	COM	COM	8'hBC		Comma control character, K28.5	r, K28.5	
	5 STP S		STP	8'hFB		Start transport packet, K27.7		
(2)	6	SDP SDP		8'h5C		Start data-link packet, K28.2		
	7	END	END	8'hFD		End of packet, K29.7		
	8	ControlChars ControlChars		\$COM, \$STP, \$SDP, \$END		Decoded control characters		
	9	LTSSM States	ltssm_state	tb.ltssm o		Enumeration of all LTSSM states possible. Bound to DUT output.	-	
	l∢ ∢ ▶ Ready	▶ config / mode variable	e / group / ધ /		[.::	

- variable declare ranges for use in cover points
- Variables may be used in this coversheet and any child coversheet

Root Block::Group Tab





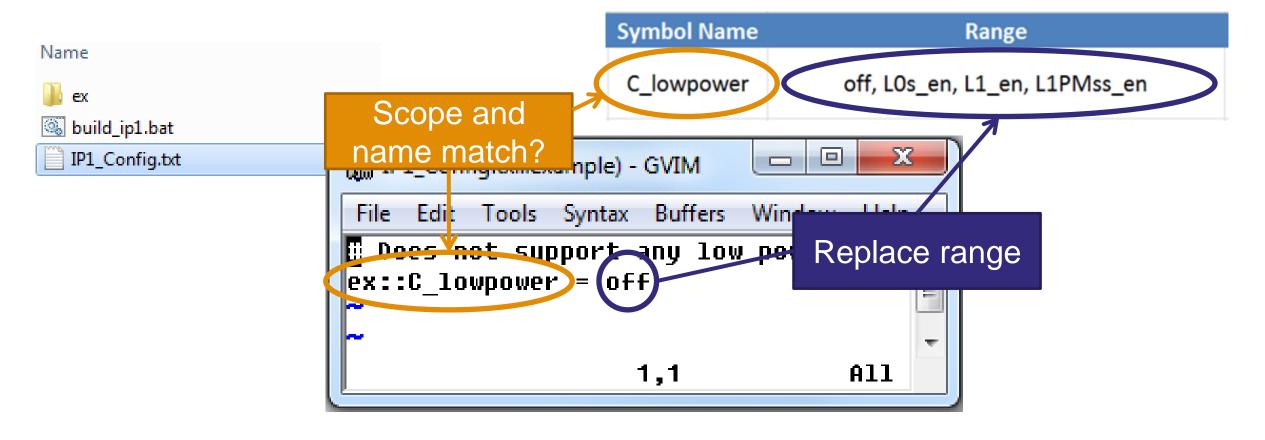


- group instantiate variables in cross-scenarios used in a covergroup
- Any mode, config, or cover variable in this or any parent coversheet

IP #1 Configuration Override



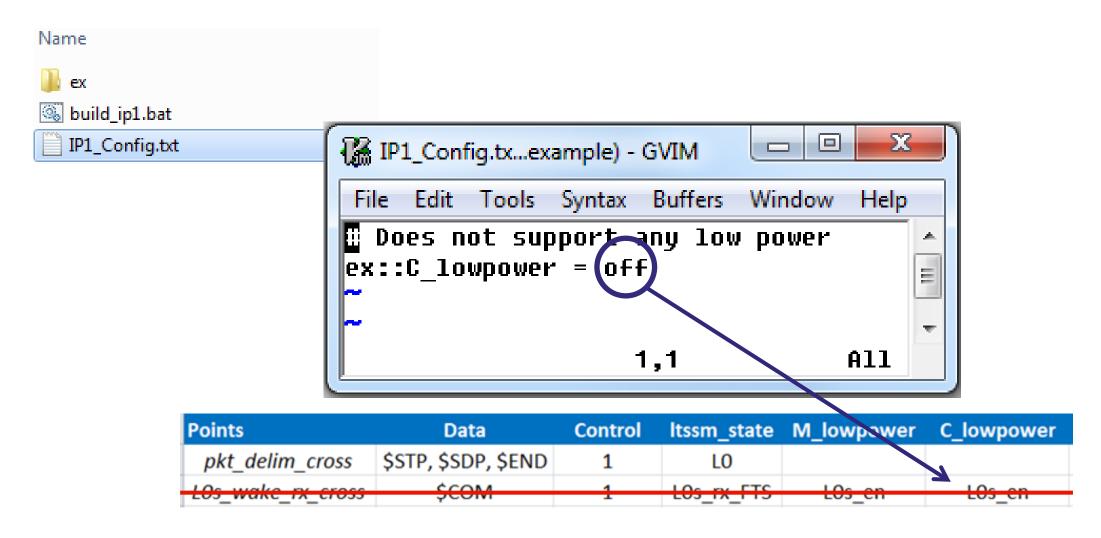




IP #1 Configuration Affect



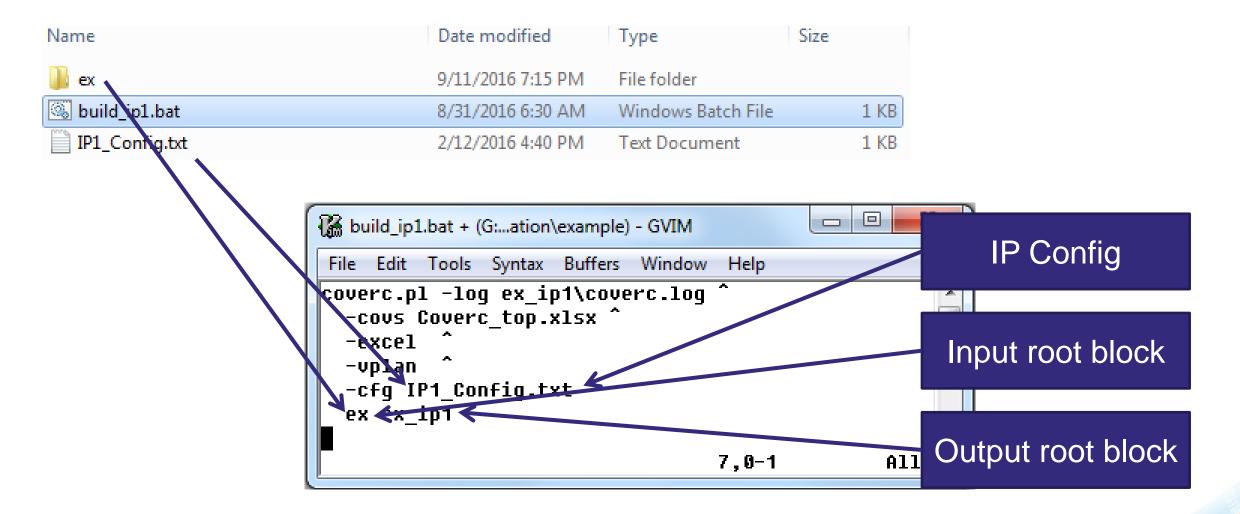




Generate Coverage for IP #1







Generated Coverage for IP #1





Name	Date modified	Туре	Size
ll ex	9/11/2016 7:15 PM	File folder	
🔐 ex_ip1	9/11/2016 10:31 PM	File folder	
build_ip1.bat	8/31/2016 6:30 AM	Windows Batch File	1 KB
IP1_Config.txt	2/12/2016 4:40 PM	Text Document	1 KB
Name	Date modified	Туре	Size
coverc.log	9/11/2016 10:13 P	M Text Document	7 KB
Coverc_top_out.xlsx	9/11/2016 10:13 P	M Microsoft Excel W.	9 KB
rx_datapath_cg.svh	9/11/2016 10:13 P	M SystemVerilog hea	4 KB
rx_datapath_toobig_cg.svh	9/11/2016 10:13 P	M SystemVerilog hea	7 KB
🛂 vplan.xml	9/11/2016 10:13 P	M XML Document	7 KB

SNUG 2016 41

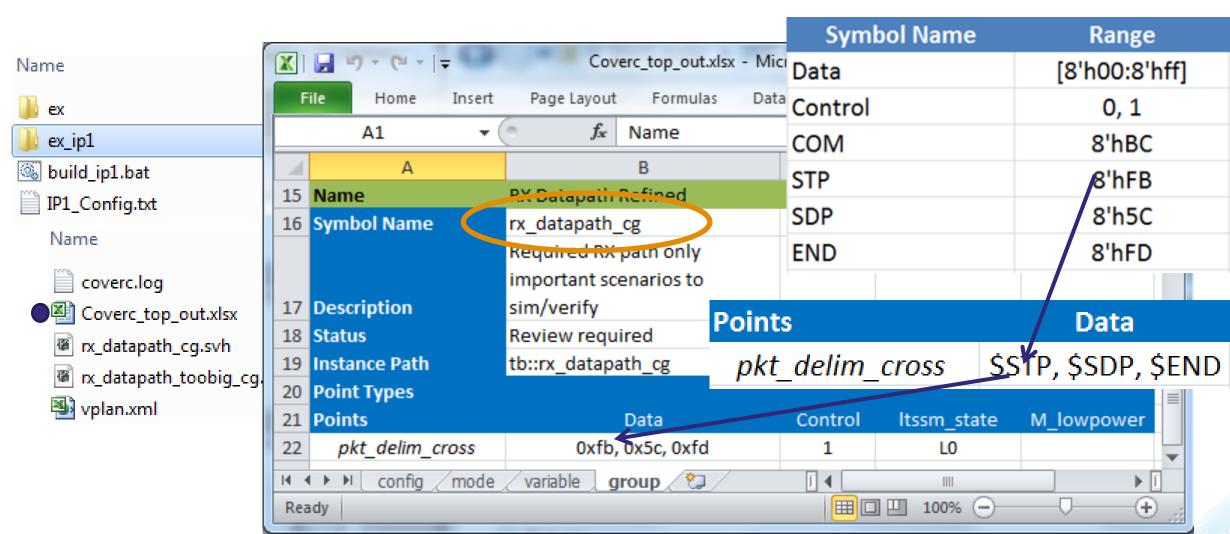




Name RUNTIME METRICS ex Number of Blocks ex_ip1 Number of Variables : 10 build_ip1.bat Number of Points Number of Signals IP1_Config.txt Number of Scenarios Number of Cross constructs: 5 Name Number of Modes Number of Configs Number of Groups coverc.log Number of External Groups: 0 Coverc_top_out.xlsx Review required Review in progress rx_datapath_cg.svh Review complete Instantiated rx_datapath_toobig_cg.svh 🗐 vplan.xml Number of Parsers Number of XLSX parsers Number of Writers Number of SV writers Number of XLSX writers Number of VPLAN writers Start time : Sun Sep 11 22:13:46 2016 End time : Sun Sep 11 22:13:46 2016 Duration











Name



ex



ex_ip1



build_ip1.bat



IP1_Config.txt

Name



coverc.log



Coverc_top_out.xlsx



rx_datapath_cg.svh



rx_datapath_toobig_cg.svh



yplan.xml

```
'ifndef RX DATAPATH CG SVH
'define RX DATAPATH CG SVH
// Class: rx datapath cq
// Required RX path only important scenarios to sim/verify
// Summary:
         Cover model scope - ex::rx_datapath_cg
         Total cover points - 3
     Total cross scenarios - 3
      Total cross constructs - 1
covergroup rx_datapath_cg;
```





Name



ex



ex_ip1



build_ip1.bat



IP1_Config.txt

Name



coverc.log



Coverc_top_out.xlsx



If it is a second of the se



| rx_datapath_toobig_cg.svh



wplan.xml

```
// Group: Cover points
// Variable: Data
// Decoded data bus from DUT
// Summary:
     Variable model scope - ex::Data
     Point model scope - ex::rx datapath cq::Data
     Point bound to
                          - signal specified at variable
                            (no port, local scope)
      Total point bins
/* int signed */ Data: coverpoint data
    bins Data 0 = { 'hfb };
    bins Data_1 = { 'h5c };
    bins Data 2 = { 'hfd };
} // coverpoint Data
```



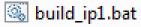


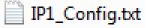
Name



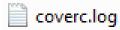








Name



- Coverc_top_out.xlsx
- rx_datapath_cg.svh
 - rx_datapath_toobig_cg.svh
 - wplan.xml

```
// Variable: Control
// Control character indication
// Summary:
      Variable model scope - ex::Control
      Point model scope
                           ex::rx datapath cq::Control
      Point bound to
                           - signal specified at variable
//
                             (no port, local scope)
      Total point bins
/* int signed */ Control: coverpoint ctrl
    bins Control 0 = { 'd1 };
} // coverpoint Control
// Variable: ltssm state
// Enumeration of all LTSSM states possible. Bound to DUT output.
//
// Summary:
      Variable model scope - ex::ltssm state
      Point model scope
                           - ex::rx datapath cq::ltssm state
      Point bound to
                           - signal specified at variable
//
//
                             (no port, hierarchical scope)
      Total point bins
/* int signed */ ltssm state: coverpoint tb.ltssm o
    bins ltssm state 0 = { L0 };
} // coverpoint ltssm state
```





Name



ex



ex_ip1



build_ip1.bat



IP1_Config.txt

Name



coverc.log



Coverc_top_out.xlsx



If it is a second of the se



rx datapath toobig cg.svh



🛂 vplan.xml

```
// Group: Crossed scenarios construct 0
    c 0: cross Data, Control, 1tssm state
        bins pkt delim cross 0 = binsof(Data.Data 0) && binsof(Control.
Control 0) && binsof(ltssm state.ltssm state 0);
        bins pkt delim cross 1 = binsof(Data.Data 1) && binsof(Control.
Control 0) && binsof(ltssm_state.ltssm_state_0);
        bins pkt delim cross 2 = binsof(Data.Data 2) && binsof(Control.
Control 0) && binsof(ltssm state.ltssm state 0);
    } // c 0: cross Data, Control, ltssm state
endgroup: rx datapath cq
`endif // RX DATAPATH CG SVH
```



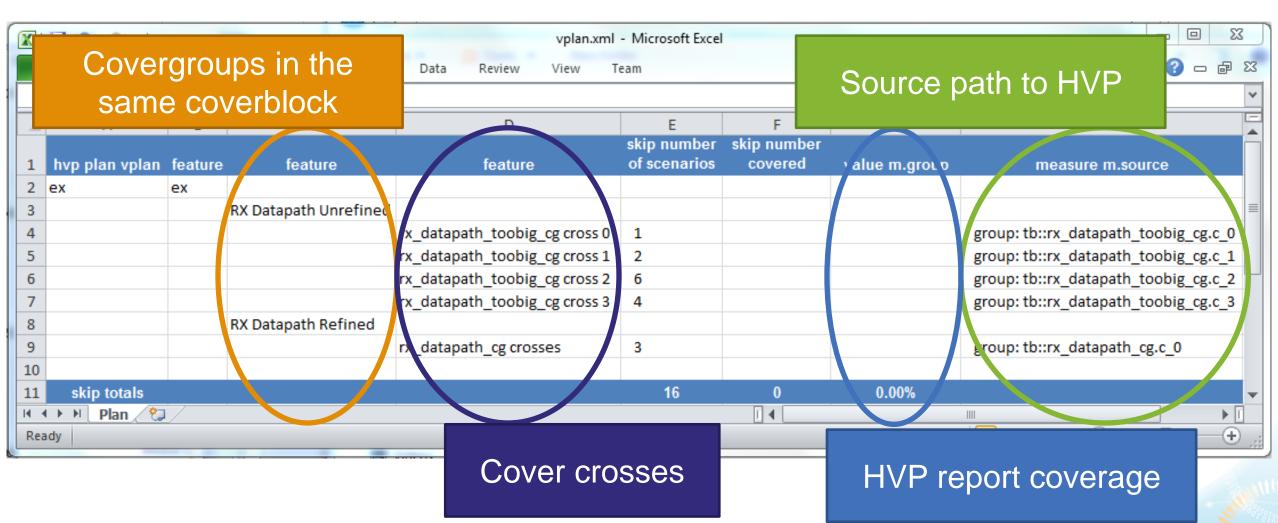


Date modified	Туре	Size
9/11/2016 7:15 PM	File folder	
9/11/2016 10:31 PM	File folder	
8/31/2016 6:30 AM	Windows Batch File	1 KB
2/12/2016 4:40 PM	Text Document	1 KB
Date modified	Type	Size
9/11/2016 10:13 PR	M Text Document	7 K
9/11/2016 10:13 PI	M Microsoft Excel W.	9 k
9/11/2016 10:13 PI	M SystemVerilog hea	4 K
9/11/2016 10:13 PI	M SystemVerilog hea	7 K
9/11/2016 10:13 Př	M XML Document	7 k
	9/11/2016 7:15 PM 9/11/2016 10:31 PM 8/31/2016 6:30 AM 2/12/2016 4:40 PM Date modified 9/11/2016 10:13 PI 9/11/2016 10:13 PI 9/11/2016 10:13 PI 9/11/2016 10:13 PI	9/11/2016 7:15 PM File folder 9/11/2016 10:31 PM File folder 8/31/2016 6:30 AM Windows Batch File 2/12/2016 4:40 PM Text Document Date modified Type 9/11/2016 10:13 PM Text Document 9/11/2016 10:13 PM Microsoft Excel W. 9/11/2016 10:13 PM SystemVerilog hea 9/11/2016 10:13 PM SystemVerilog hea 9/11/2016 10:13 PM SystemVerilog hea

SNUG 2016 48











Name	Date modified	Type	Size
	9/11/2016 7:15 PM	File folder	
ex_ip1	9/11/2016 10:31 PM	File folder	
build_ip1.bat	8/31/2016 6:30 AM	Windows Batch File	1 KB
IP1_Config.txt	2/12/2016 4:40 PM	Text Document	1 KB
Name	Date modified	Туре	Size
coverc.log	9/11/2016 10:13 P	M Text Document	7 KB
Coverc_top_out.xlsx	9/11/2016 10:13 P	M Microsoft Excel W	. 9 KB
rx_datapath_cg.svh	9/11/2016 10:13 P	M SystemVerilog hea.	4 KB
Ix_datapath_toobig_cg.svh	9/11/2016 10:13 P	M SystemVerilog hea.	7 KB
🛂 vplan.xml	9/11/2016 10:13 P	M XML Document	7 KB

Demos upon request!

Conclusions





- Handling functional coverage for highly configurable IP is HARD
 - Coverpoints are not in a vacuum
 - Static configuration
 - Dynamic mode-of-operation
- This is one solution we have employed in:
 - 2 programs (currently active)
 - 7 customers (so far)
 - Up to 2 at one time (so far)





Thank You

